A New GaAs Power MESFET Structure for Improved Power Capabilities

KLAUS FRICKE, VIKTOR KROZER, AND HANS L. HARTNAGEL, SENIOR MEMBER, IEEE

Abstract—A new GaAs power MESFET structure incorporating an additional transmission line parallel to the gate allows an increase of the single gate width by a factor of approximately 4. It is experimentally shown that the power capabilities of the new device increase correspondingly if the transmission line is properly terminated. The larger unit gate width results in a significantly higher input resistance.

I. Introduction

In current research on microwave and millimeter-wave GaAs MESFET's and MODFET's, the maximum unit gate width is restricted by the high attenuation on the gate electrode. This is because of the small cross section of the gate electrode. Therefore, various technological steps and design structures have been proposed in the literature to overcome this difficulty. New structures for the gate line have been proposed [1], [8]–[11], and technological procedures [2]–[6] have led to improved performance.

In this paper we demonstrate that a significant improvement of the gate mode attenuation is obtained by a transmission line parallel to the gate, which has to be suitably terminated. The reduced attenuation allows a much wider single gate (a factor of 4 is possible) and a corresponding improvement of the total output power of a power MESFET. It is shown that this approach leads to higher gain and cutoff frequency. An additional advantage of the new MESFET structure is its higher input resistance relative to a device with equal total gate width but more gates in parallel. This results in simpler matching circuits of greater bandwidth. The presented single-gate structure can be connected in parallel to further increase the total output power.

The optimization of MESFET device structure and topology is not only important for power applications; it also yields better performance at higher frequencies because of the reduction in noise figure and an increase in gain.

The fabricated new MESFET device incorporates a via hole grounded source and a recessed gate structure in order to improve the device performance by reducing the source resistance and inductance and by achieving excellent thermal conductivity [2], [3]. The device is designed for parallelling without crossovers.

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The authors are with the Institut für Hochfrequenztechnik, Technische Hochschule Darmstadt, Merckstr. 25, D-6100 Darmstadt, West Germany.

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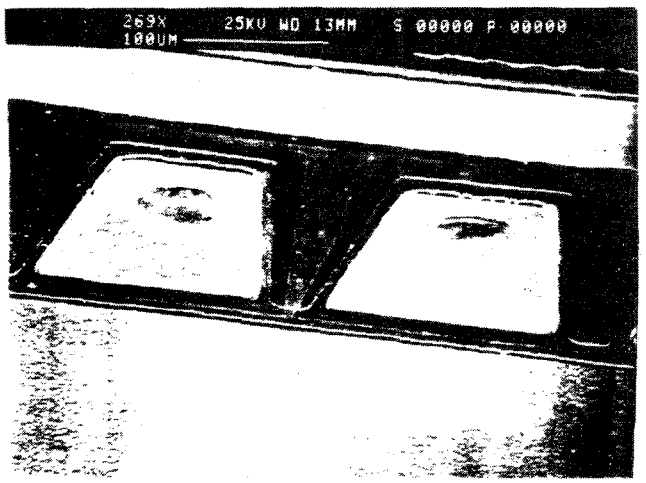
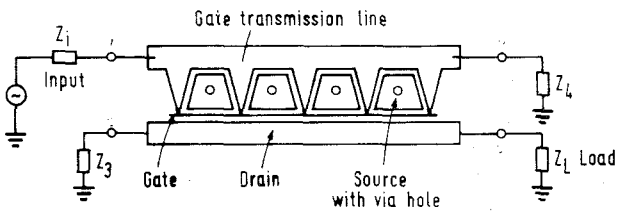


(a)



(b)

Fig. 1. (a) SEM micrograph of two segments of the improved power MESFET. Two via holes are visible in the source areas. (b) Schematic measurement setup of a FET with four segments. The ends of gate and drain electrodes are terminated by $Z3$ and $Z4$ ($|\Gamma 3| = |\Gamma 4| = 1$).

The new structure of the MESFET device will next be described, together with the most important features in topology and technological processing. Hereafter, we will present small-signal as well as large-signal experimental results for the gain, output power, and intermodulation distortion behavior of the realized GaAs MESFET structures as a function of frequency, input power, termination, and gate width. All experimental results will be fully discussed and the main conclusions will be outlined in detail. Furthermore, the advantages and potential application of the proposed structure will be given.

II. New Device Structure and Technology

The novel structure, as indicated in Fig. 1, employs a transmission line parallel to the active area of the gate to reduce the losses of this electrode. This transmission line is

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connected to the gate at every 200-μm-wide section of the gate. The now isolated source pads are grounded by via holes. Connecting pads terminate each end of the gate and drain electrodes. GaAs MESFET's with two to ten sections corresponding to gate widths ranging from 0.4 to 2 mm were fabricated. The gate length was chosen to be 2 μm in order to achieve good reproducibility. The key point of the investigation was to study the principle of the additional transmission line. Therefore, the larger gate length is useful because it yields better accuracy of the measurement results at the corresponding lower operating frequencies.

The fabrication on VPE-grown GaAs with an active layer doping of $10^{17}/cm^3$ can be described as follows. As a first step the via holes were etched in the 80-μm-thick substrate with a H_3PO_4-based etchant [12] and subsequently gold plated. This, in connection with the plated heat sink, results in an excellent thermal resistivity of 20 K/W for the 1-mm-wide device. After the mesa structure has been defined, the Au–Ge–Ni ohmic contacts were evaporated and annealed in a forming gas atmosphere at 465°C. The gate was recessed and metallized in the same photoresist step. The final saturation current was 250 mA/mm. A Ti–Pt–Au metallization contact has been chosen for the gate electrode. Finally, drain, source, and the gate transmission lines were gold plated with a thickness of 2 μm.

III. Experimental Characterization of the Device

In order to test the microwave performance of the new device structure and reveal the capabilities of the transistor device, we have constructed a specially designed four-port microstrip transistor test fixture with all calibration standards needed. The new test fixture allows access to all four ports of the transistor.

The effect of the additional transmission line can be evaluated by four-port scattering parameter measurements with a subsequent calculation of the wave parameters with a new method [14]. This method gives the values of the propagation constants, the wave impedances on the gate and drain electrodes, and the coupling coefficients of the gate and drain modes. The measurements showed that the gate mode attenuation constant α of the improved device at 4 GHz is as low as 2.3 dB/mm, whereas a conventional device without the additional transmission line has an α of approximately 7.5 dB/mm at this frequency. As a consequence, the unit gate width of a GaAs MESFET can be increased by a factor of approximately 3. Similarly the phase shift along the gate electrode dropped by a factor of 5. Due to this effect the device appears electrically shorter than a conventional one.

The maximum available gain (MAG) has been measured for several devices with various gate widths (Fig. 2) and with the two ports, numbered 3 and 4 in Fig. 1, open ended. The remaining two ports were matched for maximum gain. The new devices are compared experimentally with a similar structure without the parallel gate line. The calculated values are obtained from a small-signal equivalent model [13] modified for distributed four-port devices [14]. The theoretical values for the various four-port devices are also indicated.

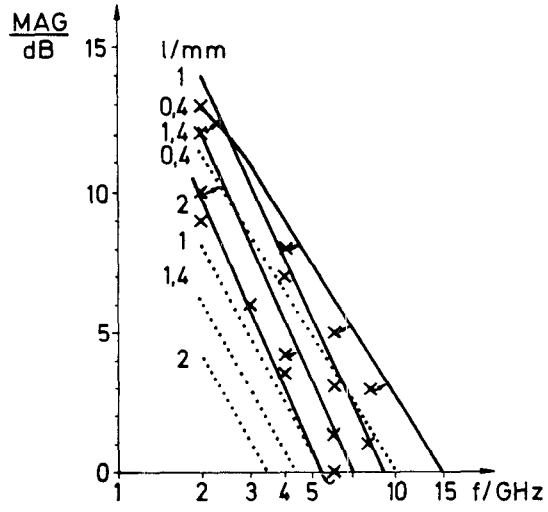

Fig. 2. Maximum available gain (MAG) versus the frequency f with the gate width l as a parameter: $\cdots$ conventional structure (calculated); ——— improved structure (calculated); $\times\times\times$ measurement (U_{DS} = 6 V, $I_D = I_{dss}/2$).

All GaAs MESFET's measured show the expected 6 dB/octave fall with increasing frequency. The largest transistor, with 2 mm single-gate width, exhibits 0 dB gain at nearly 5.5 GHz. We can well observe that the microwave performance of the structure without the parallel gate transmission line increasingly deteriorates with larger gate widths. Even the MESFET with a gate width of only 400 μm exhibits better performance than its counterpart without an additional parallel gate transmission line.

The real part of the input impedance is of paramount importance for matching the device. The improved structure with 2 mm unit gate width shows an optimum input resistance normalized to the gate width of 20 $\Omega \cdot$mm whereas the 1-mm-wide single-gate structure exhibits 13 $\Omega \cdot$mm in the range of 4 to 8 GHz.

Fig. 3 summarizes the results obtained for the microwave performance of the new transistor structure. For this measurement ports 3 and 4 are kept open ended. The behavior of MAG, output power at 1 dB compression point ($P_{1\ dB}$), and the power-added efficiency at the 1 dB compression point can be inferred from Fig. 3 as a function of the gate width for the new transistor structure. A closer view of the values reveals that for these particular devices with gate length of 2 μm and all technological parameters equal to those described previously, the optimum gate width is 1 mm. At this gate width the parallel gate transmission line clearly compensates for the losses introduced by the 2 μm single-gate electrode. Larger single-gate widths introduce excessive losses, which diminish the attainable power and efficiency. Similar results have been obtained by other authors [5], [11]. However, we shall demonstrate below that an appropriate termination at the free end of the gate line can considerably enhance the performance of the devices with larger single-gate

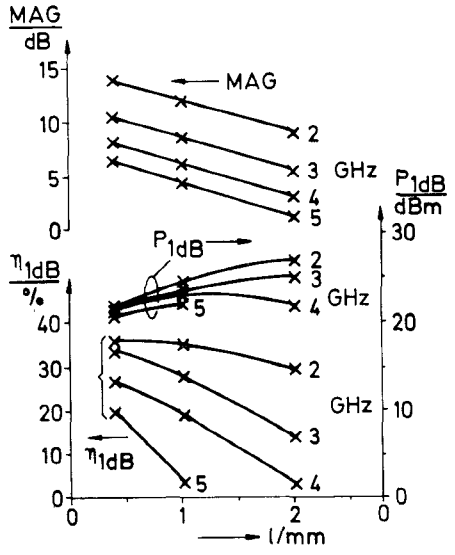

Fig. 3. Maximum available gain (MAG), power at the 1 dB compression point ($P_{1\ dB}$) and power-added efficiency ($\eta_{1\ dB}$) versus the gate width l of the improved structure Parameter frequency f (Z_3, Z_4 open circuit); ($U_{DS} = 6$ V, $I_D = I_{dss}/2$).

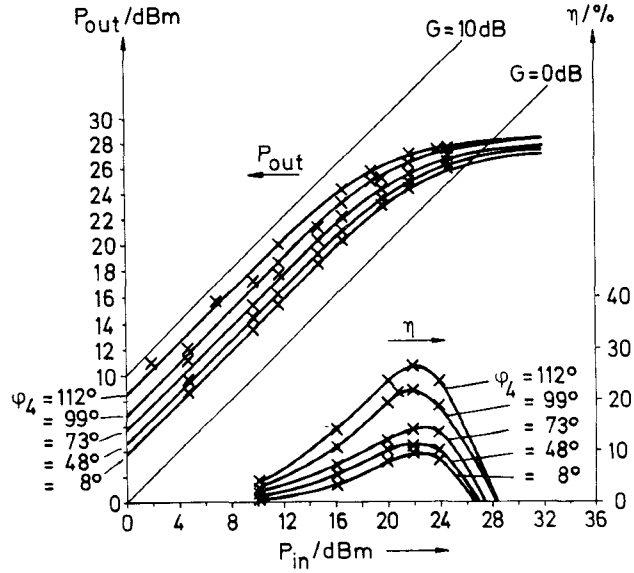

Fig. 4. Output power (P_{out}) and power added efficiency (η) as a function of the input power (P_{in}) with the phase ϕ_4 of the reflection coefficient $\Gamma 4$ as a parameter. $|\Gamma 4| = 1$. $f = 3.91$ GHz ($U_{DS} = 6$ V, $I_D = I_{dss}/2$)

widths. Thus, higher output power and MAG versus single-gate width can be obtained incorporating the technique of termination of ports 3 and 4 with suitable loads.

The 2 mm device has been chosen for further characterization of its power capabilities. Fig. 4 shows the output power and the power-added efficiency versus input power at 3.91 GHz. At this frequency the gain of the GaAs MESFET has already fallen below 4 dB with ports 3 and 4 at the end of the drain and the gate open ended, respectively. However, as is also indicated in Fig. 4, we have connected the free end of the gate line (port 4), after accomplishing matching, to a purely imaginary load of variable value. Thus, the parameter in Fig. 4 is the phase of the reflection coefficient seen at port 4 with the magnitude of the reflection coefficient equal to unity. We can observe a substantial increase in gain and in power-added efficiency in Fig. 4 as the phase is varied. We have found that an inductive termination at port 4 improves the overall gain performance by 3 dB and the power-added efficiency by a factor of 3, while a capacitive termination even reduces the gain. It has to be emphasized that this gain increase does not affect the conjugate complex match at the input and the output of the transistor device. Hence, we can conclude that an open termination of the gate line is not the optimum choice for this transistor structure. However, we can furthermore observe that the change in saturating power is only marginal when the termination at port 4 is varied. Consequently the variation of the phase of the reflection coefficient at port 4 is restricted to the small-signal region and shows less effect in the power capabilities of the device. Remarkable in this context is also that the higher output power due to the increased gain yields a significant increase in power-added efficiency. We can thus increase the gain–bandwidth product of the MESFET by correctly terminating port 4 of the gate line. A closer view of Fig. 2 reveals that by this means the MAG of the device with 2 mm single-gate width improved to that of the 1 mm single-gate width device with ports 3 and 4 open ended. Though, it is obvious that the 2 mm device delivers more power than the 1 mm one. Consequently, we have also increased the power–bandwidth product per millimeter gate width. We also point out that the phase of the reflection coefficient $\Gamma 4$ for optimum device performance is not dependent on gate bias voltage and is constant for a wide band of frequencies. This means that, once the optimum value for the termination at port 4 has been found experimentally or theoretically from the design structure, this termination does not need to be changed and consequently can be incorporated in the same substrate as the transistor device. This is of great relevance for MMIC applications.

A comprehensive experimental confirmation of the capabilities incorporating the above results is summarized in Fig. 5 for the 2 mm MESFET structure. In this figure the dependence of MAG, the saturated output power with matching for maximum gain and maximum power, the output power at 1 dB compression point, and the power-added efficiency are drawn as a function of the phase of the reflection coefficient at port 4. An inductive termination is suitable for obtaining maximum MAG and power-added efficiency, which reach values of approximately 8 dB and 28 percent, respectively, at 3.91 GHz compared with the 4 dB and 9 percent with open-ended gate line at port 4. These values are even superior to those obtained with the 1 mm transistor device at the same frequency and open-ended gate line. Furthermore, as indicated above, the increase in output power is only marginal for different reflection coefficient phases. This result does not change even if we match the transistor for maximum output power.

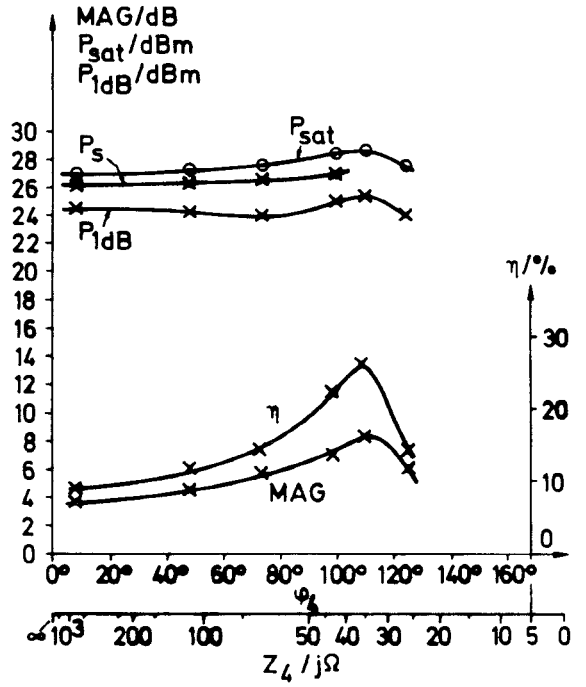

Fig. 5. Maximum available gain (*MAG*), power added efficiency (η), power at the 1 dB compression point ($P_{1\,dB}$), saturation power (P_s, tuned for optimum gain), and saturation power (P_{sat}, tuned for optimum power) versus the phase ϕ_4 of the reflection coefficient $\Gamma 4$ ($Z4$): $f = 3.91$ GHz ($U_{DS} = 6$ V, $I_D = I_{dss}/2$).

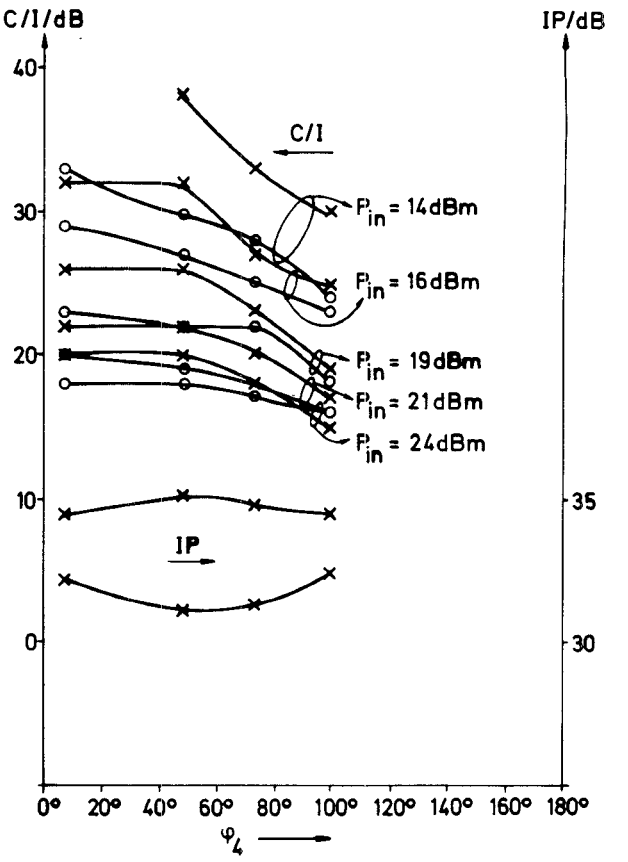

Fig. 6. Carrier to intermodulation ratio (C/I) and third-order intercept point IP versus the phase ϕ_4 of the reflection coefficient $\Gamma 4$ with the input power P_{in} as a parameter. $f = 3.91$ GHz; ∘ tuned for maximum output power; × tuned for maximum gain ($U_{DS} = 6$ V, $I_D = I_{dss}/2$).

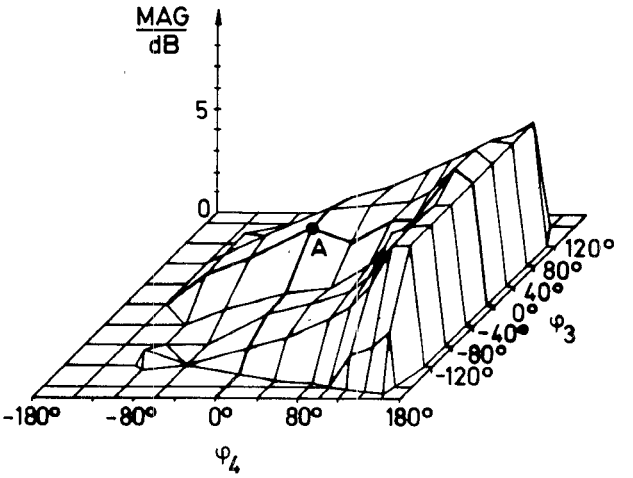

Fig. 7. Maximum available gain (*MAG*) versus the phases of the reflection coefficients $\Gamma 3$ and $\Gamma 4$ at 4 GHz. Point *A* indicates the conventional termination. ($U_{DS} = 6$ V, $I_D = I_{dss}/2$).

As far as the intermodulation distortion is concerned Fig. 6 illustrates the variation of the carrier/intermodulation ratio (C/I) and the intercept point with matching for maximum saturated power and gain respectively as a function of the phase of the reflection coefficient at port 4. The intercept point varies only by approximately 2 dB for different values of the phase of the reflection coefficient. The curves for C/I yield that matching for maximum output power is always superior to that for *MAG* and is more pronounced at lower input power levels. We may then conclude that the increase in gain achievable through appropriate termination also increases the value of the nonlinear products generated by the transistor in the output power spectrum.

It is interesting to note that the gate tuning has the most significant effect on *MAG*, as indicated in Fig. 7, whereas the variation of the phase of the reflection coefficient at port 3 is somewhat less pronounced. Also remarkable is the large variation possibility of the phase of the reflection coefficient at port 3, without having a great influence on *MAG*. This aspect and the strong correlation between the phase of the reflection coefficient at port 3 and the drain matching support the conclusion that the drain electrode can be regarded as a lumped element. Observe that the gain increases steadily as the phase of the reflection coefficient at port 4 is changed from capacitive to inductive terminations, regardless of the values realized by the termination at port 3. In particular, for some optimum values *MAG* exceeds the values obtained with conventional circuitry, indicated as point *A* in Fig. 7. Finally, the variation of the intermodulation distortion product and of the intercept point as a function of drain termination has been investigated experimentally and the results are shown in Fig. 8. We have already mentioned above that the open end termination at port 3 yields the best results for *MAG*, maximum saturated power, and intermodulation distortion. In Fig. 8 the gate line end has been terminated in the optimum phase of the reflection coefficient.

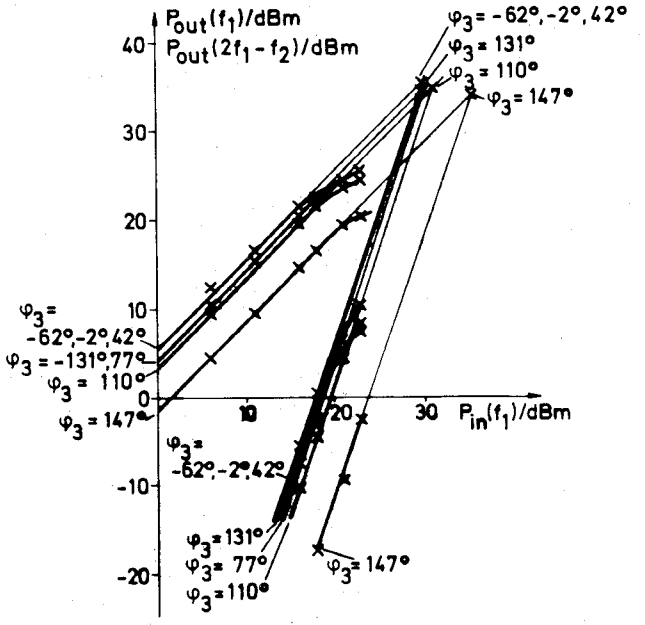

Fig. 8. Output power P_{out} at the fundamental f_1 and the intermodulation frequency $2f_1 - f_2$ as a function of the input power P_{in} at the fundamental with the phase ϕ_3 of the reflection coefficient $\Gamma 3$ as a parameter. $|\Gamma 3| = 1$. $f_1 = 3.91$ GHz, $f_2 = 3.92$ GHz ($U_{DS} = 6$ V, $I_D = I_{dss}/2$).

IV. Conclusions

We have presented a promising design for microwave and millimeter-wave GaAs MESFET's and MODFET's in order to overcome the limitations imposed by the gate attenuation and packaging densities. Gate line attenuation has been diminished by introducing an additional transmission line in parallel to the gate electrode, which feeds the large single gate at several points. For optimum performance the gate transmission line has to be terminated by an inductive load. With this procedure single gate widths of up to 2 mm have been realized with a gate length of 2 μm. These devices exhibit nearly 1 W at 4 GHz. Because of the single gate structure, there have been no problems arising from the low input impedance which is usually observed when several MESFET's are connected in parallel in order to achieve such large gate widths.

In particular, the termination at the end of the gate line has a significant influence on overall transistor performance. Terminating the otherwise free end of the gate line by an inductive load increased the *MAG* by 3 dB and the power-added efficiency by a factor of 3. The maximum values obtained at 4 GHz are for the gain (8 dB) and for the power-added efficiency (28 percent in class A operation). Furthermore, we have observed that the optimum termination does not change with operating point and frequency of operation. We can then conclude that this technique can successfully be exploited for increasing the gain–bandwidth product of the MESFET's. The output power and the intercept point did not change significantly for different terminations at ports 3 and 4.

The termination at port 3 could be of some importance for MMIC design, in order to accomplish final tuning to the drain matching circuit directly on the wafer.

The transistor structure allows the incorporation of a large number of low-inductance and low-thermal-resistance via holes. It is designed to be paralleled without additional crossovers to achieve larger output powers.

The results presented above are especially important for millimeter-wave power applications because of the reduced gate attenuation and larger achievable single-gate widths.

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Klaus Fricke was born in Munich, West Germany, in 1957. He received the Dipl.-Ing. degree in electrical engineering from the Technical University of Darmstadt, Darmstadt, West Germany, in 1983.

Since October 1983, he has been employed at the Institute of High Frequency Electronics at the Technical University of Darmstadt, where he was engaged in studies of technological improvements of GaAs power MESFET's. Since receiving the Ph.D. degree, in 1988, he has been involved in the design of high-temperature GaAs circuits and sensors.

Viktor Krozer was born in Leningard, U.S.S.R., in 1958. He received the Dipl.-Ing. degree in electrical engineering from the Technical University of Darmstadt, Darmstadt, West Germany, in 1984.

From 1985 until 1986 he was a visiting scientist at the European Space Operations Center, Darmstadt, West Germany. Since 1986, he has been employed at the Institute of High Frequency Electronics at the Technical University of Darmstadt, where he is working toward the Ph.D. degree in the area of nonlinear circuits and large-signal analysis.

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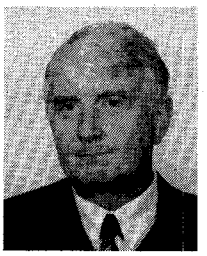
Hans L. Hartnagel (SM'72) was born in Geldern, Germany, in 1934. He received the Dipl.-Ing. degree in 1960 from the Technical University of Aachen, Aachen, West Germany, and the Ph.D. and Dr.Eng. degrees



from the University of Sheffield, England, in 1964 and 1971, respectively.

After having worked for a short period with Telefunken in Ulm, West Germany, he joined the Institut National des Sciences Appliquées, Villeurbane, Rhône, France. He then joined the University of Sheffield as a Senior Research Assistant. In October 1962, he became a Lecturer and later became a Senior Lecturer and Reader. In January 1971 he became a Professor of Electronic Engineering at the University of Newcastle upon Tyne, England. Since October 1978 he has been the Professor of High-Frequency Electronics at the Technical University of Darmstadt, Darmstadt, West Germany.

Dr. Hartnagel is the author of several books and numerous scientific papers on microwave tubes, microwave semiconductor devices, and their technology and circuits. He has held many consulting positions, partly while on temporary leave of absence from his university positions.